Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further clarify Applicants disclosed and claimed invention.

Support for the amendments is found in the original claims including the Figures 3H and 3I and in the Specification at paragraph 0053:

"As shown in Figure 3G, a second (top) dielectric layer 50 is deposited over the assembly shown in Figure 3F to provide a substantially planar surface overlying the electrically redistribution traces 48. The second dielectric layer 50 may be made of any suitable material known to those skilled in the art, including spin-on polyimide or BCB. As shown in Figure 3E, a second set of vias 52 are formed in the second dielectric layer 50 wherein each via 52 is aligned with an associated redistribution trace 48. The second set of vias 52 may be formed by standard photoresist patternization and etching techniques known to those skilled in the art. Thereafter, **electrically conductive bumps 54**, for example, solder, gold, silver, nickel, tin containing bumps, **are formed on the assembly with each solder bond extending through the vias 52 formed in the second dielectric layer 50 and makes electrical connection to the redistribution trace 48.** Additional metallization layers may be

interposed between the electrically conductive bump 54 and the redistribution trace 48. The electrically conductive bump 54 may be formed by any manner formed to those skilled in the art, including, for example but not limited to, placing balls over the vias 52, stenciling, or plating and subsequent reflow."

No new matter has been added.

Claim Objections

Claim 39 has been listed as cancelled to overcome Examiner objection.

Claim Rejections under 35 USC 102

1. Claims 1-8, 11, 14, 19-22, 25, 28, 33-36, and 38 stand rejected under 35 USC 102(e) as being anticipated by Chua et al. (6,825,553).

Chua et al. discloses a packaging system for a multi-chip multi-layer system where chip die are placed in cavities formed in a separate substrate with redistribution layers over the multi-chip configuration terminating in electrical connections such as conductive bumps or balls (see Abstract). Chua et al.

form saw segments from the substrate to include multiple die having different function to form a "system on a chip packaging solution" (col 3, lines 31-35; col 8, lines 44-59).

Chua et al. disclose **using silicon, ceramics or other suitable material as the substrate** (col 5, lines 36-56) and teach forming the cavities **by an anisotropic etching process** (col 5, lines 48-49). In a first embodiment, Chua et al. also teach coating the top surface of the substrate with a **die attach material, which may include epoxy resins, polyimides, and benzocyclobutene(BCB)** (col 5, lines 57-67; item 112, Figure 1B). In the first embodiment, the die with attached balls are placed upside down so that the **balls fit within the cavities in the substrate cavities which have been filled with die attached material** (col 6, lines 1-29).

In a second embodiment, Chua et al. disclose forming **cavities (by anisotropic etching) in a silicon substrate** where the cavities are about the size of an individual dies ant the bottom of the cavities is coated with a die attach material (adhesive) (including polyimide or BCB) (item 218, Figure 2B; col 7, lines 15-35). **An undisclosed type of dielectric layer is then formed over the die in the cavities** by spin or spray coating including filling gaps between the substrate and die. Vias are

then formed to expose bond pads on the dies and a metallization layer (redistribution layer) is formed on the dielectric layer to connect to the bond pads through the vias (col 7, lines 38-65). Chua et al. disclose that the metallization layer may be **formed of aluminum or copper "or other metals known in the art"** (col 8, lines 1-10) and that the bond pads may be treated with undisclosed underbump metallization prior to forming the metallization layer to improve adhesion.

Chua et al. also teach forming vias in an uppermost **dielectric layer (undisclosed type)** (over metallization layers) where **solder balls** or other conductive bumps are formed **within the openings** to connect to the underlying metallization layers (col 4, lines 65-68; col 8, lines 31-39; item 320, Figure 3F).

Thus, Chua et al. fail to teach several aspects of Applicants disclosed and claimed invention including with respect to claims 1, 20, and 34:

"forming a first dielectric layer over the first surface of the chip carrier substrate and over the integrated circuit chip in each of the cavities **wherein the first dielectric layer comprises at least one of a polyimide and BCB.**"

With respect to claims 5, 20, and 34, Chua et al. also fail to teach:

"wherein each electrically **conductive bump overlies the second dielectric layer and comprises an unrounded portion extending into one of the vias formed in the second dielectric layer** and so that the electrically conductive bump is electrically connected to one of the redistribution traces."

Thus, Chua et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor*

Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim Rejections under 35 USC 103

2. Claims 13, 16, 18, 27, 30, 32, 37, and 41 stand rejected under 35 USC 103(a) as being unpatentable over Chua et al., above.

Applicants reiterate the comments made above with respect to Chua et al., and note that in the **adhesive material** (PCB or polyimide) is **disclosed to fill the cavities** in the first embodiment, within which already formed balls on a separate chip are subsequently fitted into.

Nowhere do Chua et al. disclose or suggest "forming a first dielectric layer over the first surface of the chip carrier substrate and over the integrated circuit chip in each of the cavities wherein the first dielectric layer comprises at least one of a polyimide and BCB."

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

A statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)*.

With respect to claims 16, 23, 30, and 41, Nowhere do Chua et al. disclose or suggest "wherein the second dielectric layer comprises at least one of a polyimide and BCB."

Rather, forming solder balls within the dielectric layer vias as taught by Chua et al. would likely deteriorate a polyimide or BCB layer and make it unsuitable for its intended purpose.

Nevertheless, Applicants disclosed and claimed material and conductive bum structure and dielectric layers are nowhere disclosed or suggested by Chua et al.

With respect to claims 18 and 32, Chua et al. merely disclose placing solder balls on bonding pads (col 2, line7) or in the via openings by an undisclosed process (col 8, lines 32-39), and therefore do not teach Applicants claimed structure or process.

3. Claims 15, 29, and 40 stand rejected under 35 USC 103(a) as being unpatentable over Chua et al., above, in view of Becker et al. (US 6,617,674).

Applicants reiterate the comments made above with respect to Chua et al.

Assuming *arguendo* a proper motivation for combination, the fact that Becker et al. disclose forming a package by forming an overlying layer of silicone except for covering bonding pads and forming metal traces with one end on the bond pad and on the surface of the silicone where the metal trace is titanium/nickel/copper and a solder ball is at the distal end of

the trace, does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claims 9, 10, 23, and 24 stand rejected under 35 USC 103(a) as being unpatentable over Chua et al., above, in view of Benavides et al. (US 6,548,895).

Applicants reiterate the comments made above with respect to Chua et al.

Even assuming *arguendo* that Benavides et al. is *analogous* art and a proper motivation for combination, that fact that Benavides et al. disclose forming **fluidic channels (trenches) in a substrate for an electro-microfluidic by a variety of material removal methods** such as "milling with a miniature milling tool, laser milling, chemical etching, or abrasive jet spray milling" **or alternatively, that parts of the microfluid device on the**

substrate can be fabricated by using additive processes, such as "rapid prototyping with built-up plastic layers, thermal spray metal deposition, cold spray deposition, Laser Engineered Net Shape (LENS.TM.) directed metal deposition, casting, **molding**, injection molding of a moldable material, cold-isostatic processing, hot isostatic processing, sintering, lamination, etc.", does not further help Examiner in producing Applicants disclosed and claimed invention.

Moreover, Examiner has not shown in the prior art that etching, molding and milling are known equivalents.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claims 12, 17, 26, and 31 (apparently) stand rejected under 35 USC 103(a) as being unpatentable over Chua et al., above, in view of Volfson et al. (US 5,106,461).

Applicants reiterate the comments made above with respect to Chua et al.

Assuming *arguendo* a proper motivation for combination, the fact that Volfson et al. disclose reactive ion etching to form vias in a dielectric layer does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The cited references, alone or in combination, fail to produce Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness with respect to Applicants independent and dependent claims.

Applicants have amended the claims to clarify their

disclosed and claimed invention and respectfully request favorable reconsideration by Examiner.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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